

In the Claims:

Please cancel claims 1-21 and 31-53 without any disclaimer and a prejudice to.

Listing of claims is as follows:

1-21. (Cancelled)

22. (Original) A thin film transistor array panel for a liquid crystal display comprising:

a gate wire formed on an insulating substrate and including a plurality of gate lines extending to a first direction, gate electrodes connected to the gate line, and gate pads connected to an end of the gate line;

a gate insulating layer having contact holes exposing the gate pad and formed in a matrix shape on the gate wire and the substrate;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the semiconductor layer and including a plurality of data lines extending to a second direction crossing the gate line, source electrodes adjacent to the gate electrode, drain electrode separated from the data line and the source electrode and located at the opposite side of the source electrode with respect to the gate electrode, and data pads connected to an end of the data line;

a conductive pattern including a plurality of first patterns formed on the source electrode and the data line, second patterns formed on the drain electrode, third patterns formed on the data pad, and pixel electrodes connected to the second pattern; and

a passivation layer formed on the conductive pattern, the semiconductor pattern and the

substrate, and having a plurality of first openings exposing the pixel electrode, second openings exposing the gate insulating layer between the two adjacent data lines, third openings located on the gate pad, and fourth openings exposing the third pattern,

wherein the data wire is only formed between the conductive pattern and the semiconductor layer, the semiconductor layer is formed on the whole gate insulating layer except for the portion under the second opening, and the portions of the semiconductor layer under the two adjacent data lines are separated from each other.

23. (Original) The thin film transistor array panel of claim 22, further comprising a contact layer formed between the semiconductor layer and the data wire to have the same layout as the data wire for reducing the contact resistance between the semiconductor layer and the data wire.

24. (Original) The thin film transistor array panel of claim 23, wherein the conductive pattern further includes a fourth pattern connected to the gate pad through the contact hole and the third opening.

25. (Original) The thin film transistor array panel of claim 23, wherein the pixel electrode is overlapping the adjacent gate line and the portion of the semiconductor layer sandwiched between the pixel electrode and the gate line is isolated from the other portion.

26. (Original) The thin film transistor array panel of claim 23, wherein the gate

insulating layer includes a first portion formed between the two gate pads and the two data pads, the passivation layer has fifth openings exposing the first portion of the gate insulating layer, and the semiconductor layer is not formed under the fifth opening.

27. (Original) The thin film transistor array panel of claim 23, the passivation layer covers the edge of the pixel electrode.

28. (Original) The thin film transistor array panel of claim 23, wherein the first opening exposes the edge of the pixel electrode.

29. (Original) The thin film transistor array panel of claim 28, further including a storage wire formed on the substrate, overlapped with the pixel electrode and covered by the gate insulating layer, wherein the portion of the semiconductor layer sandwiched between the storage wire and the pixel electrode is isolated from the other portion.

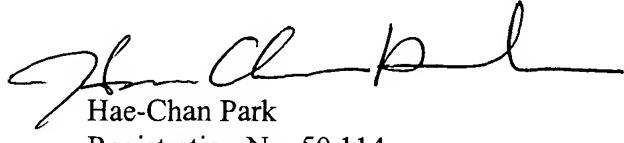
30. (Original) The thin film transistor array panel of claim 28, wherein the conductive pattern is made of indium-tin-oxide.

31 – 53. (Cancelled)

Conclusion

It is respectfully requested that this amendment be entered prior to the examination of the above-referenced patent application. It is believed that no new matter is added by this amendment. By this amendment, claims 22-30 are pending, among which claims 22 is an independent claim. If the Examiner desires any additional information, the Examiner is invited to contact applicants' attorney at the telephone number listed below to expedite prosecution.

Respectfully submitted,



Hae-Chan Park
Registration No. 50,114

Date: August 21, 2003

MC GUIREWOODS, LLP
1750 Tysons Boulevard
Suite 1800
McLean, VA 22102-4215
(703) 712-5365 (Direct Phone)
(703) 712-5280 (Direct Fax)

\COM\218493.1